

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of

NEVILL

Atty. Ref.: 550-244

Serial No. 09/887,561

TC/A.U.: 2122

Filed: June 25, 2001

Examiner: Tang, K.

For: INTERCALLING BETWEEN NATIVE AND NON-NATIVE  
INSTRUCTION SETS

\* \* \* \* \*

June 3, 2004

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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Sir:

Technology Center 2100

**INFORMATION DISCLOSURE STATEMENT**

As suggested by 37 C.F.R. 1.97, the undersigned attorney brings to the attention of the Patent and Trademark Office the references listed on the attached form PTO-1449, a copy of each of which is enclosed. This is not to be construed as a representation that a search has been made or that no better prior art exists, or that a reference is relevant merely because cited.

The Examiner is requested to initial the attached form PTO-1449 and to return a copy of the initialed document to the undersigned as an indication that the attached references have been considered and made of record.

The requisite fee of \$180.00 to is included.

Respectfully submitted,

**NIXON & VANDERHYE P.C.**

By:

  
John R. Lastova  
Reg. No. 33,149

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NEVILL

Serial No. 09/887,561

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<b>INFORMATION DISCLOSURE CITATION</b>  (Use several sheets if necessary)	ATTY. DOCKET NO.	SERIAL NO.
	550-244	09/887,561
	APPLICANT	
	NEVILL	
	FILING DATE	TC/A.U.
	June 25, 2001	2122

## **U.S. PATENT DOCUMENTS**

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## **FOREIGN PATENT DOCUMENTS**

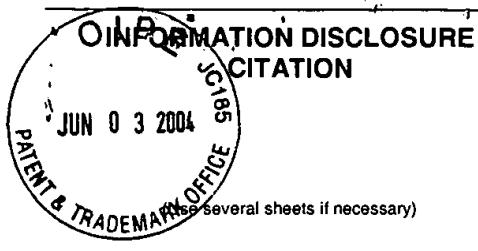
**OTHER DOCUMENTS (including Author, Title, Date, Pertinent pages, etc.)**

	IBM Technical Disclosure Bulletin, March 1988, pp 308-309, "System/370 Emulator Assist Processor For a Reduced Instruction Set Computer".
	IBM Technical Disclosure Bulletin, July 1986, pp 548-549, "Full Function Series/1 Instruction Set Emulator".
	IBM Technical Disclosure Bulletin, March 1994, pp 605-606, "Real-Time CISC Architecture HW Emulator On A RISC Processor".
	IBM Technical Disclosure Bulletin, March 1998, p272, "Performance Improvement Using An EMULATION Control Block".
	IBM Technical Disclosure Bulletin, January 1995, pp537-540, "Fast Instruction Decode For Code Emulation on Reduced Instruction Set Computer/Cycles Systems".
	IBM Technical Disclosure Bulletin, February 1993, pp231-234, "High Performance Dual Architecture Processor".

\*Examiner

### Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.



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	550-244	09/887,561
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the book ARM System Architecture by S. Furber.
the book Computer Architecture: A Quantitative Approach by Hennessy et al.
the book The Java Virtual Machine Specification by Tim Lindholm et al., 1 <sup>st</sup> and 2 <sup>nd</sup> editions.

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